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Claims:

1. A data transmission link for transmitting time-sensitive data, said link including a first node (10) connected to a plurality of end nodes (30) by a broadband packet-switched network (1), whereby each end node (30) is connected to at least one end terminal (40),
each of said end nodes (30) including:
timing generation circuitry (350, 360, 370) adapted to generate an output timing signal that is phase locked to a received reference timing signal originating at said first node (10),
means (380) for receiving data structure information from said first node (10) and identifying a data structure format from said information for transmitting time-sensitive data between said end nodes (30) and said end terminals (40),
a delay signal generator (320) for generating a delay signal in response to delay information received from said first node (10), and
data conversion means (340) communicating with said delay signal generating means (320), said data structure receiving means (380) and said timing generation circuitry (350, 360, 370), said data conversion means being arranged to receive payload data from said first node (10) and retransmit payload data identified as time-sensitive data in a synchronous manner to said end terminal, wherein the timing of said payload data transmission is adjusted in each end node on the basis of said received timing signal, said received data structure format and said received delay signal, such that all end nodes transmit said payload data substantially simultaneously.

2. A link as claimed in claim 1, wherein at least one intermediate node is arranged between said first node (10) and at least one of said end nodes (30), each said intermediate node including timing generation circuitry (50, 60) adapted to generate an output timing signal that is phase locked to a received reference timing signal originating at said first node (10), and to propagate said output timing signal to said end node (30).

3. A link as claimed in claim 1 or 2, wherein said means (310) for receiving data structure information from said first node (10) further includes means (310) for extracting a data transmission start time marker from said information, said data transmission start marker indicating an absolute start to transmit time for transmitting time-sensitive data between said end nodes (30) and said end terminals (40).

4. A link as claimed in claim 3, wherein said delay signal generator (320) is arranged to adjust the timing of said transmission start time marker by said generated delay.

5. A link as claimed in any previous claim, wherein each said end node (30) is arranged to determine a node transmission delay between said end node (30) and said first node (10) and to communicate this node transmission delay to said first node (10), and wherein said first node (10) is arranged to determine the maximum node transmission delay from each end node (30) and communicate this maximum node transmission delay to all end nodes (30) as delay information.

6. A link as claimed in claim 5, wherein said node transmission delay is the round-trip delay between and end node (30) and said first node (10).

7. A link as claimed in any previous claim, wherein said timing generation

circuitry includes means (50) for extracting a timing reference from a received signal, means (71, 72, 73; 350, 360, 370) for phase locking a generated timing signal to said timing reference and means (60) for imposing said phase locked timing signal on an output signal to generate said output timing signal.

8. A link as claimed in any previous claim, wherein said network is an Ethernet.

9. A method for transmitting time-sensitive data through a packet-switched network between a first node (10) and a plurality of end nodes (30), wherein each end node (30) is connected to at least one end terminal (40) said method including:
propagating a timing signal through said network from said first node to each said end nodes,
transmitting a signal indicative of a data structure type from the first node to each end node, said data structure type identifying the data format for transmission from said end node to said end terminals,
transmitting a delay figure from said first node to each end node, said delay figure being indicative of the maximum transmission delay between said first node and any one of said end nodes,
transmitting payload data between said first node and said end terminals, whereby the payload data transmitted between each end node and the corresponding end terminal is formatted in said identified data structure format in accordance with said timing signal and adjusted in dependence on said delay figure such that payload data transmission from each end node to each end terminal occurs substantially synchronously.

10. A method as claimed in claim 9, further including the step of generating said delay figure by determining a maximum transmission delay

between any end node and said first node.

11. A method as claimed in claim 10, further including the step of sending a delay message from an end node to said first node and returning the delay message to the end node, calculating a transmission delay based on the return time of said message, and communicating this transmission delay to said first node.

12. A method as claimed in any one of claims 9 to 11, wherein said step of transmitting a signal indicative of a data structure type includes transmitting a burst of information messages, wherein the interval between each information message is indicative of the transmission repetition rate of the identified data structure from said end node to said terminals.

13. A method as claimed in claim 12, further including the step of:
in each end node, determining the interval between each information message, generating a periodic timing marker corresponding to said interval and utilising said timing marker to commence transmission of an identified data structure of payload data to said end terminal.

14. A method as claimed in claim 13, further including the step of:
in each end node adjusting said periodic timing marker in dependence on said delay figure.

15. A node for use in a broadband packet-switched network adapted to receive packet switched-data in a first format from a sending node in said network and transmit synchronous data to an end terminal (40) located outside said network in a second format, said node (30) including
timing generation circuitry (350, 360, 370) adapted to generate an output signal timing signal that is phase locked to a received reference timing

signal,

means (380) for receiving data structure information indicative of the data structure and repetition rate of said second format,

a delay signal generator (320) for generating a delay signal in response to delay information received from said first node (10), and

data conversion means (340) communicating with said delay signal generating means (320), said data structure receiving means (380) and said timing generation circuitry (350, 360, 370), said data conversion means being adapted to receive payload data in said first data format and retransmit payload data identified as time-sensitive data in said second format, wherein the timing of said payload data transmission is adjusted on the basis of said received timing signal, said received data structure format and said received delay signal.

16. A node as claimed in claim 15, further including means (320, 310, 330) for identifying start of data received in said first format, wherein said start of data represents the start of a unit of payload data to be transmitted in said second format.

17. A node as claimed in claim 15 or 16, wherein said means (310) for receiving data structure information from said first node (10) further includes means (310) for extracting a data transmission start time marker from said information, said data transmission start marker indicating an absolute start to transmit time for transmitting time-sensitive data between said end nodes (30) and said end terminals (40).

18. A node as claimed in claim 17, wherein said delay signal generator (320) is arranged to adjust the timing of said transmission start time marker by said generated delay.

19. A node as claimed in any one of claims 15 to 18, wherein said node is further adapted to determine a node transmission delay from said sending node (10)

20. A node as claimed in claim 19, wherein said node transmission delay is the round-trip delay between said node and said sending node (10).

21. A node as claimed in any one of claims 15 to 20, wherein said timing generation circuitry includes means (50) for extracting a timing reference from a received signal, means for phase locking a generated timing signal to said timing reference (61, 62, 70; 350, 360, 370) and means (60) for imposing said phase locked timing signal on an output signal to generate said output timing signal.